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EXAMINER	
KANG, DONGHEE	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/001,625	PIO, FEDERICO
	Examiner	Art Unit
	Donghee Kang	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-15 and 17-20* is/are rejected.

7)☒ Claim(s) *4 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/405,506* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. This application appears to be a division of Application No. 09/405,506, filed 23 September 1999. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth only that portion of the earlier disclosure which is germane to the invention as claimed in the divisional application.

Information Disclosure Statement

2. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field 24 October 2001.

Claim Objections

3. Claim **15** is objected to because of the following informalities:

Claim 15 recites the limitation "**the second conductive region**" and "**a second conductive region**" in lines 10 & 16, respectively. One of them should have different phrase because they are not same conductive region. The examiner suggests that "a second conductive region" changes to - -a third conductive region--. The phrase "the second conductive region" should be - -a second conductive region" because there is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required. The examiner interprets "a second conductive region" as a third conductive region.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **1–3, 5, 15 & 18** are rejected under 35 U.S.C. 102(b) as being anticipated by Jiang et al. (US 5,773,314).

Regarding claim **1**, Jiang et al. teach a method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising (Figs.2-8):

forming a first conductive region (34,Fig.2; Col.4, lines 14-16) inside a substrate of semiconductor material (30); forming a first insulating region (42; Col.4, lines 33-34) of dielectric material above the first conductive region; forming a first through region (44) of electrically conductive material inside the first insulating region, and in direct contact with the first conductive region; forming a second conductive region (48b;Fig.6) above the first insulating region (42), in a position not aligned and not in contact with the first through region (44); forming a second insulating region (58, Fig.7; Col.7, lines 44-45) of dielectric material, covering the second conductive region; forming, inside the second insulating region (58), a second through region (60; Col.7, lines 46-47) of electrically

conductive material, extending as far as the first through region, aligned and in direct electrical contact with the first through region; and

forming, above the second insulating region, a third conductive region (62; Fig.8) aligned and in direct electrical contact with the second through region (60).

Regarding claim **2**, Jiang et al. teach the first (44) and second (60) through regions having a substantially cross-sectional dimension (Fig.8).

Regarding claim **3**, Jiang et al. teach the step of forming the first conductive region (34) comprising the step of introducing doping ion species inside the substrate (Col.4, lines 15-16).

Regarding claim **5**, Jiang et al. teach the second and the third conductive regions formed in successive metal levels (Fig.8).

Regarding claim **15**, Jiang et al. teach a method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising (Figs.2-8):

forming a first conductive region (34,Fig.2; Col.4, lines 14-16) inside a substrate of semiconductor material (30); forming a first insulating region (42; Col.4, lines 33-34) on the first conductive region; forming a first opening completely through the first insulating region, thereby exposing the first conductive region (Col.4, lines 54-57); forming a first through region (44) by filling the first opening with electrically conductive material to directly contact the first conductive region; forming a second conductive region (48b;Fig.6) above the first insulating region (42), in a position not aligned and not in contact with the first through region (44); forming a second insulating region (58, Fig.7; Col.7, lines 44-45) on the second conductive region and the first insulating region;

forming a second opening completely through the second insulating region, thereby exposing the first through region (Col.7, line 47-48); forming a second through region (60; Col.7, lines 46-47) by filling the second opening with electrically conductive material to directly contact the first through region; and

forming, above the second insulating region, a third conductive region (62; Fig.8) aligned and in direct electrical contact with the second through region (60).

Regarding claim **17**, Jiang et al. teach the second and the third conductive regions formed in successive metal levels (Fig.8).

6. Claims **9 & 12** are rejected under 35 U.S.C. 102(e) as being anticipated by Bandyopadhyay et al. (US 5,854,515).

Regarding claim **9**, Bandyopadhyay et al. teach a method of forming a semiconductor structure electrically coupling two conductive regions separated by at least twp insulating layers, comprising (Figs. 3-10 &Col.5, line 5 – Col.6, line 34):

forming a first conductive region (28, Fig.3); forming a first insulating layer (26, Fig.4) having an upper surface over the first conductive region (28); etching a first opening (54, Fig.5) through the first insulating layer to expose a portion of the first conductive region; forming a first conductive plug (34, Fig.6) that fills the first opening and is electrically coupled to the first conductive region (28), the first conductive plug (34) having an upper surface extending no further than the upper surface of the first insulating layer (26); forming a second insulating layer (22, Fig.7) having an upper surface over the first insulating layer (26); etching a second opening (58, Fig.8) through

the second insulating layer to expose a portion of the upper surface of the first conductive plug (34); forming a second conductive plug (32, Fig.9) that fills the second opening (58) and is electrically coupled to the first conductive plug (34), the second conductive plug directly contacting the upper surface of the first conductive plug and further having an upper surface extending no further than the upper surface of the second insulating layer (22); and forming a second conductive region (14c, Fig.10) over the second insulating layer (22), the second conductive region being electrically coupled to the first conductive region (28) through the first (34) and second (32) conductive plugs (Col.6, lines27-33).

Regarding claim **12**, Bandyopadhyay et al. teach forming the first conductive plug comprises (Fig.6):

depositing a conductive layer (56) over the first insulating layer and filling the first opening (Col.5, lines 41-48); and

removing the conductive layer over the first insulating layer by polishing to leaving conductive material filling the first conductive via (Col.5, lines 48-53).

7. Claim **9** is rejected under 35 U.S.C. 102(e) as being anticipated by Pasch et al. (US 6,239,491).

Pasch et al. teach a method of forming a semiconductor structure electrically coupling two conductive regions separated by at least two insulating layers, comprising (Fig.1 & Col.1, line 50 - Col.2, line 33):

forming a first conductive region (10); forming a first insulating layer (30) having an upper surface over the first conductive region (10); etching a first opening (32) through the first insulating layer to expose a portion of the first conductive region (Col.1, line 66); forming a first conductive plug (44) that fills the first opening and is electrically coupled to the first conductive region (Col.2, lines 1-2), the first conductive plug (44) having an upper surface extending no further than the upper surface of the first insulating layer (30); forming a second insulating layer (50) having an upper surface over the first insulating layer (30); etching a second opening (52) through the second insulating layer to expose a portion of the upper surface of the first conductive plug44); forming a second conductive plug (Col.2, line 25-26) that fills the second opening and is electrically coupled to the first conductive plug (44), the second conductive plug directly contacting the upper surface of the first conductive plug and further having an upper surface extending no further than the upper surface of the second insulating layer (50); and forming a second conductive region (60a) over the second insulating layer (50), the second conductive region being electrically coupled to the first conductive region (10) through the first and second conductive plugs.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **6-7 & 18-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 5,773,314) in view of Lee et al. (US 6,165,839).

Regarding claims **6 & 18**, Jang et al. applies to claim 1 explained above.

Jiang et al. do not teach that the first insulating region comprises a first insulating layer of a first dielectric material, and a second insulating layer of a second dielectric material, superimposed on each other, the step of forming the first through region comprises, in succession, the steps of etching the second dielectric material with first etching parameters, etching the first dielectric material with second etching parameters, thereby forming a through aperture in the first insulating region, and filling the through aperture with the electrically conductive material.

Lee et al. in Figs. 2-4 teach that the first insulating region comprises a first insulating layer of a first dielectric material (9; Col.3, line 40), and a second insulating layer of a second dielectric material (10; Col.3, line 45), superimposed on each other, the step of forming the first through region comprises, in succession, the steps of etching the second dielectric material with first etching parameters using CF_4-SF_6 as an etchant, etching the first dielectric material with second etching parameters using CHF_3 as an etchant (Col.3, lines 50-53), thereby forming a through aperture in the first insulating region, and filling the through aperture with the electrically conductive material.

Therefore, it would have been obvious to one of ordinary skill in the art of making semiconductor device to apply the teachings of Lee et al. in the method of Jiang et al. to show using a different etching parameters for different dielectric materials in order to

obtain a high etch rate and a vertical sidewalls in the opening formed in the first insulating region.

Regarding claim **7 & 19**, Jiang et al. do not teach that the first dielectric material comprises silicon oxide and the second dielectric material comprises silicon nitride. It is recognized in the art that the preferred etch stop material is silicon nitride because its properties are well known, and it is currently used for semiconductor fabrication. The preferred underlying layer is silicon oxide or BPSG. Note that Lee et al. also teach the first insulating region comprising a silicon oxide (9, SiO_2; Col.3, line 40), and a second insulating layer comprising silicon nitride (10, Si_3N_4; Col.3, line 45) served as an etch stop layer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the first insulating region having a silicon oxide and silicon nitride as taught by Lee into the Jiang's device in order to provide an etch stop layer. When a conductive plug is formed using a chemical mechanical polishing (CMP) process, the surface of the conductive plug can be substantially flush with the surface of the silicon nitride film. This invention allows for the stacking of vias to further reduce the integrated circuit area.

10. Claims **6, 8, 18 & 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 5,773,314) in view of Yaung et al. (US 6,165,880).

Regarding claims **6 & 18**, Jang et al. applies to claim 1 explained above.

Jiang et al. do not teach that the first insulating region comprises a first insulating layer of a first dielectric material, and a second insulating layer of a second dielectric material, superimposed on each other, the step of forming the first through region comprises, in succession, the steps of etching the second dielectric material with first etching parameters, etching the first dielectric material with second etching parameters, thereby forming a through aperture in the first insulating region, and filling the through aperture with the electrically conductive material.

Yaung et al. in Figs. 1-3 teach that the first insulating region comprises a first insulating layer of a first dielectric material (20, Si_3N_4; Col.5, line 18), and a second insulating layer of a second dielectric material (22, SiO_2; Col.5, line 24), superimposed on each other, the step of forming the first through region comprises, in succession, the steps of etching the second dielectric material with first etching parameters using C_4F_8, CH_3F & etching parameters as an etchant (Col.5, lines 42-44), etching the first dielectric material with second etching parameters using C_4F_8, CH_3F as an etchant (Col.5, lines 50-54), thereby forming a through aperture in the first insulating region, and filling the through aperture with the electrically conductive material.

Therefore, it would have been obvious to one of ordinary skill in the art of making semiconductor device to apply the teachings of Yaung et al. in the method of Jiang et al., to show using a different etching parameters for different dielectric materials in order to obtain a high etch rate for the silicon oxide layer, a vertical sidewalls in the opening, and a high selectivity of the silicon oxide layer being etched down to the silicon nitride layer.

Regarding claims **8 & 20**, Jiang et al. do not teach that the first dielectric material comprises silicon nitride and the second dielectric material comprises silicon oxide. It is recognized in the art that the preferred etch stop material is silicon nitride because its properties are well known, and it is currently used for semiconductor fabrication. The preferred superjacent layer is silicon oxide or BPSG. Note that Yaung et al. also teach the first insulating region comprising a silicon nitride (20; Col.5, line 18), and a second insulating layer comprising silicon oxide (22; Col.5, line 24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the first insulating region having a silicon nitride and silicon oxide as taught by Yaung into the Jiang's device to provide an etch stop layer because this etch stop layer acts to protect structures underlying the etch stop layer from damage due to the chemical etch of the silicon oxide layer.

11. Claim **10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Pasch et al. (US 6,239,491) in view of S. Wolf (Silicon Processing, Vol.1 – Processing Technology, pp.280-282).

Pasch et al. teach the first conductive region (10) formed in the substrate. However, Pasch et al. do not explicitly teach that forming the first conductive region comprises implanting a dopant into a substrate. Wolf notes that ion implantation is primarily used to add dopant ions into the surface of silicon wafers and has a several advantages, such as ability to more precisely control the number of implanted dopant atoms into substrate (see page 282). Wolf also teaches using ion implantation to form

source/drain regions (see Table 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use ion implantation method to form a conductive region, such as source/drain region, in a substrate of Pasch et al. as disclosed by Wolf since ion implantation has ability to more precisely control the number of implanted dopant atoms into substrate to obtain a desired doping concentration.

12. Claims **11 & 13-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bandyopadhyay et al. in view of Tsui (US 5,891,799).

Regarding claim **11**, Bandyopadhyay et al. teach that forming the first conductive region (28) comprises depositing a conductive material, such as tungsten or aluminum, prior to forming the first insulating layer (26). Bandyopadhyay et al. do not teach the conductive material comprising a semiconductor material. Tsui teaches the conductive material (12) including a semiconductor material, such as a doped polysilicon (Col.5, lines 5-8). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the metal material of Bandyopadhyay et al. with a doped polysilicon as taught by Tsui, since a doping concentration and doping conductivity type can be easily changed in polysilicon to obtain a desired conductivity type and/or concentration.

Regarding claims **13 & 14**, Bandyopadhyay et al. teach substantially the entire claimed invention, as applied to claim 9 explained above, except that forming the second insulating layer comprises:

forming a first dielectric layer over the first conductive region; and forming a second dielectric layer over the first dielectric layer,

wherein the second insulating layer comprises etching through the second dielectric layer and subsequently etching the first dielectric layer.

However, Tsui teaches in Fig.11 & Col.7, lines 1-22 that forming the second insulating layer comprises forming a first dielectric layer (SiO_2, 14') over the first conductive region (12); and forming a second dielectric layer (Si_3N_4, 16') over the first dielectric layer (14'), wherein the second insulating layer comprises etching through the second dielectric layer (16') and subsequently etching the first dielectric layer (14') to form a via hole in which a patterned second conductive plug (4') is later formed for the next level of metal line.

Therefore it would have been obvious to one of ordinary skill in the art of making semiconductor device to apply the teaching of Tsui in the method of Bandyopadhyay et al., to form a silicon nitride layer on the silicon oxide layer in order to provide an etch stop layer when the second conductive plug is formed by a chemical mechanical polishing (CMP) process so that the surface of the second conductive plug can be substantially flush with the surface of the silicon nitride film. This invention allows for the stacking of vias to further reduce the integrated circuit area.

Allowable Subject Matter

13. Claims **4 & 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art reference, taken along or in combination, do not teach or render obvious that the first conductive region is of metal material, a third insulating region extends above the substrate, and the first conductive region extends above the third insulating region.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang
Patent Examiner

dhk
January 27, 2003